

Hores | Login | Logout | Access information | Ateris | Purchase

REER KPLORE GUIDE

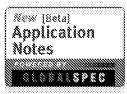
Welcome United States Patent and Trademark Office

Search Results SEARCH SEARCH

Your search matched 36 of 1776775 documents.

A maximum of 36 results are displayed, 25 to a page, sorted by Relevance in Descending order.

Results for "(((pipeline)<in>metadata)<and>((bank)<in>metadata))<and>((performance..."



Search Options
 View Session History
 New Search
 Key

IEEE Journal or Magazine
IEET Journal or Magazine

NET Conference Proceeding

IEEE Conference Proceeding

HEER SYD IEEE Standard

RESERVAN

(((pip	(((pipeline) <in>metadata) <and> ((bank)<in>metadata))<and> ((performance)<in></in></and></in></and></in>				
	21 1 1				
2)	эпеск то	o search only within this results set			
Dispis	y Form	et: Citation Citation & Abstract			
	15	EEE/IET Books Educational Courses			
ICCC	UET iou	reals transactions letters magazines conference proceedings and standards			
1000	IE I Jou	rnals, transactions, letters, magazines, conference proceedings, and standards.			
r vis	w se	sected items Select All Deselect All			
****	26.	Speculation techniques for improving load related instruction scheduling Yoaz, A.; Erez, M.; Ronen, R.; Jourdan, S.;			
		Computer Architecture, 1999. Proceedings of the 26th international Symposium on			
		2-4 May 1999 Page(s):42 - 53			
		Digital Object Identifier 10.1109/ISCA.1999.765938			
		AbstractPtus Full Text: PDF(212 KB) IEEE CNF			
		Elights and Permissions			
	27.	Architecture and performance of the Hitachi SR2201 massively parallel processor system Fujii, H.; Yasuda, Y.; Akashi, H.; Inagami, Y.; Koga, M.; Ishihara, O.; Kashiyama, M.; Wada, H.; Sumimo			
		Parallel Processing Symposium, 1997, Proceedings, 11th International			
		1-5 April 1997 Page(s):233 - 241			
		Digital Object Identifier 10.1109/IPPS.1997.580901			
		AbstractPlus Full Text: PDF(836 KB) REE ONF			
		Rights and Permissions			
	28.	Predictive sequential associative cache Calder, B.; Grunwald, D.; Emer, J.;			
		High-Performance Computer Architecture, 1996. Proceedings. Second international Symposium on			
		3-7 Feb. 1996 Page(s):244 - 253			
		Digital Object Identifier 10.1109/HPCA.1996.501190			
		AbstractPtus Full Text: PDF(1132 KB) RESE ONF Bights and Permissions			
		Trighte and 1 stringsource			
m	29.	A 300 MIPS, 300 MFLOPS four-issue CMOS superscalar microprocessor			
		Ikumi, N.; Tanaka, S.; Sawada, K.; Nagamatsu, M.; Kondo, Y.; Takayanagi, T.; Minagawa, K.; Akiba, H.			
		Rodman, P.; Bratt, J.; Man Kit Tang; Nofal, M.; Joshi, C.; Scanlon, J.; Solid-State Circuits Conference, 1984, Digest of Technical Papers, 41st ISSCC., 1994 IEEE Internation			
		16-18 Feb. 1994 Page(s):204 - 205			
		Digital Object Identifier 10.1109/ISSCC.1994.344669			
		AbstractPlus Full Text: PDF(216 KB) RESE ONF			
		Rights and Permissions			
unn;	30.	Software pipelining for Jetpipeline architecture			
	30.				
		Katahira, M.; Sasaki, T.; Hong Shen; Kobayashi, H.; Nakamura, T.;			

Rights and Permissions

14-16 Dec. 1994 Page(s):127 - 134

Digital Object Identifier 10.1109/ISPAN.1994.367155

AbstractPlus | Full Text: PDF(392 KB) | IEEE CARE

31.	Differential register bank design for self timed differential bipolar technology Jackson, D.L.; Kelly, R.; Brackenbury, L.E.M.;
	Circuits, Devices and Systems, IEE Proceedings -
	Volume 144, <u>Issue 5</u> , Oct. 1997 Page(s):297 - 302
	AbstractPtus Full Text: PDF(720 KB) HEY JNC
32.	Banked multiported register files for high-frequency superscalar microprocessors Tseng, J.H.; Asanovic, K.;
	Computer Architecture, 2003. Proceedings, 30th Annual International Symposium on 9-11 June 2003 Page(s):62 - 71
	Digital Object Identifier 10.1109/ISCA.2003.1206989
	AbstractPtus Full Text: PDF (300 KB) ISSE ONF Rights and Permissions
33.	Reducing register ports for higher speed and lower energy Park, I.; Powell, M.D.; Vijaykumar, T.N.;
	Microarchitecture, 2002. (MiCRO-35). Proceedings, 35th Annual IEEE/ACM International Symposium on 18-22 Nov. 2002 Page(s):171 - 182
	Digital Object Identifier 10.1109/MICRO.2002.1176248
	AbstractPlus Full Text: PDF(277 KB) HEE CRS Rights and Permissions
34.	Implementation of RNS analysis and synthesis filter banks for the orthogonal discrete wavelet trans Ramirez, J.; Garcia, A.; Parrilla, L.; Lloris, A.; Fernandez, P.G.;
	Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on
	Volume 3, 8-11 Aug. 2000 Page(s):1170 - 1173 vol.3
	Digital Object Identifier 10.1109/MWSCAS.2000.951423
	AbstractPlus Full Text: PDF (352 KB) HEEE ONF
	Rights and Permissions
35.	The impact of memory organization on the performance of matrix multiplication Hake, JF.; Homberg, W.;
	Supercomputing '90. Proceedings of
	12-16 Nov. 1990 Page(s):34 - 40
	Digital Object Identifier 10.1109/SUPERC.1990.129999
	AbstractPlus Full Text: PDF(460 KB) RESE CRS
	Rights and Permissions
36.	Parallel computation of neural networks in a processor pipeline with partially shared memory Okawa, Y.; Suyama, H.;
	Tools for Artificial Intelligence, 1990., Proceedings of the 2nd International IEEE Conference on
	6-9 Nov. 1990 Page(s):276 - 282
	Digital Object Identifier 10.1109/TAI.1990.130347
	AbstractPlus Full Text: PDF(420 KB) IEEE CNF
	Rights and Permissions

Inspec

Help Cor